C: Remarks:

The present amendment is filed formally in accordance with the examiner's suggestions which are appreciated and to place this application in condition for allowance. The examiner is thanked for the suggestions. The second Claim 27 was RENUMBERED 31 AND CANCELED because the subject matter was moved into claim 1. As required by the Examiner, Figure 8 has been added to particularly illustrate the case of claim 9, and corresponding changes have been made in the specification. Figure 9 illustrates particularly the subject matter of claims 26 and 27 and when combined with Figure 10, Figures 9 and 10 illustrate particularly Claims 15, 16, 17 and 18. Corresponding changes have been made in the description.

In answer to the examiners question about the use of purge in the claim, which use was correct, and to answer the examiner's question it has been decided to combine the duplicate second claim 27 into claim 1, as that language is true for all claims and makes the use of purge in claim 1 clear to the person of ordinary skill in the art. Indeed purging occurs even though the moving of a coherency region from one set of processing nodes to another effectively leaves behind cache entries on the old nodes and that cache entries for the same main storage address will not be established in the new nodes until the old entries are invalidated.

Morioka et al (6,631,447) was cited by the Examiner but the invention here obtained benefits which this reference attempted to achieve but the applicant's claimed invention solved the attempt without the exercise of manipulation. The reference has limitations which required manipulation of page table information that is cached in the TLB.

The claimed invention is focused on using the dispatch of virtual processors for controlling the size and extent of a required coherency domain and achieves this by directly changing coherency bits.

Morioka did not teach the use of virtual processor dispatch and focused only on manipulation of page table information that is cached in the TLB. Morioka detailed description does not give any indication that they foresaw the claimed use of the virtual processor management to more efficiently control the cache coherency domains.

This invention is much more direct, the control program can change the coherency boundaries directly by changing the "Coherency Mode Bits" as claimed in claim 1, with future specifics in dependent claims. The claimed invention does not require the intermediate steps of changing page tables and manipulating TLB entries.

Morioka limitations:

They use TLB to hold the information which defines whether an address requires a global coherency search.

- the applicants' claimed invention does not use the TLB for this function (much less hardware area is required)

- since Morioka uses the TLB it needs to modify hundreds or thousands of TLB entries when the coherence boundaries are dynamically changed.

They use Page Table Entries (PTE) to hold the same information (LCC/GCC). This requires a larger PTE, our invention does not require this.

Figure 5 of Morioka clearly shows the limitation of that earlier patent. The LCC/GCC determination comes from the TLB. The

Cluster ID No (311) is static, there is no indication in Morioka that the Cluster ID number would be changed after an initial setup.

This patent application of the applicants here shows how to have an adjustable system. Putting the LCC/GCC indication in the TLB entries makes adjustments difficult as in Morioka, while this application's solution is different and better.

Take the Morioka example of changing a partition from LCC to GCC as the processing needs for that partition grows. In the applicants' invention they simply dispatch the workload with the wider scope (see page 4 paragraph 37). The same change of coherency boundaries using Morioka requires change to the page table settings and selective purging/updating of the TL Bs.

As to the second reference, the Hagersten patent that the examiner points to (6226671) seems not to have a Figure 2 with elements 30A and 30B which the examiner used as the reason for his rejection.. Thus the claims are not understood. Clarification is requested. Nevertheless, the claims have been amended, so a new reconsideration of Hagersten 6226671 is required, as Hagersten does not deal with changing coherency boundaries directly with coherency mode bits nor does he suggest a system with the advances of the claims as amended.

REPLACEMENT SHEETs are submitted for the first three Figures of drawings and NEW SHEETs are submitted for the required new drawings 8, 9 and 10. The supporting text is inserted on page 15 of the specification.

Accompanying this Amendment is a Terminal Disclaimer for this application disclaiming any term after the expiration of the related patent application USSN 10/603,251 when it issues as a patent.

A notice of allowance is respectfully requested.

RESPECTFULLY SUBMITTED
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Annotated Sheet



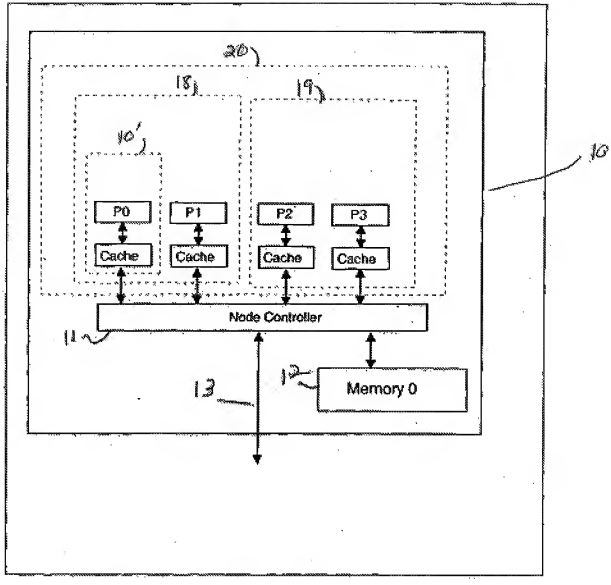


FIGURE 1.

Annotated Sheet



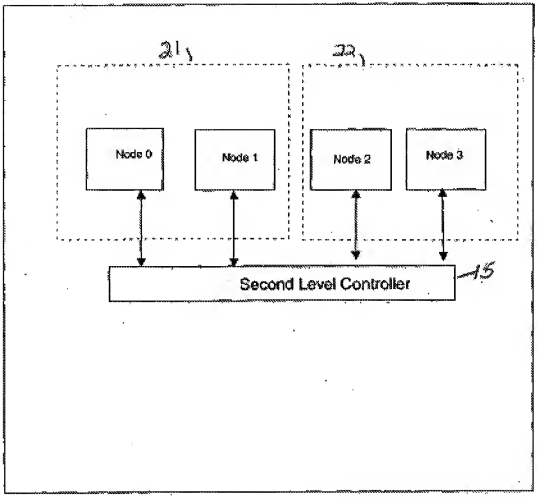


FIGURE 2.

Annotated Sheet



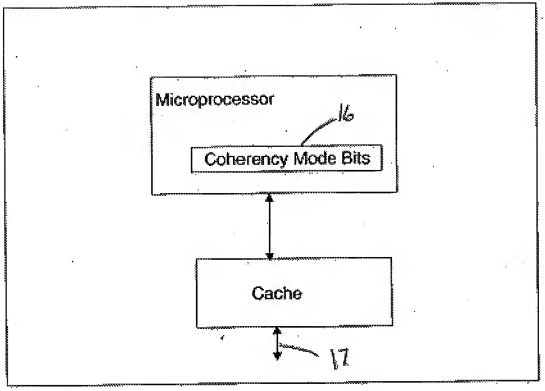


FIGURE 3.